In order to clarify the claims, Applicant has deleted the second impurity directional recitations from the claims.[1] Accordingly, it is respectfully submitted that this objection has been rendered moot, and it is requested that it be withdrawn.

Claim Rejections - 35 USC §103

The Examiner also rejects Claims 1, 3, 15, 18, 21, 24, 27-34 and 42-48 under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Ko et al. and/or Mikoshiba. This rejection is respectfully traversed.

The present invention, as recited in the amended independent claims, requires that the impurity region be formed under the channel forming region and the source region.

Applicants do not believe that this feature is shown in any of the cited references. For example, Chang et al. shows in Figs. 1(b) and 1(c) an impurity region 18 under a channel region and LDD regions 14. It is not formed under the source or drain regions 16. Further, Applicants respectfully submit that the impurity region cannot be formed under the source or drain regions as a silicide layer 17 is formed on the source and drain regions and operates as a mask during formation of the impurity regions. See Col. 3, lns. 46-54 in Chang et al.

Hence, because none of the references disclose or suggest this claimed feature of the present invention, the claims are patentable over the cited references. Accordingly, it is requested that the rejections thereover be withdrawn.

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[1] Applicants are adding independent Claim 56 which recites the second impurity being introduced in the direction of the < 110 > axis but does not recite a diagonal direction limitation.

New Claims

Applicants are adding new Claims 56-59 herewith. These claims are directed to an EL display device in order to distinguish over the cited references.

If any fee is due for these new claims, please charge our deposit account 50/1039.

Conclusion

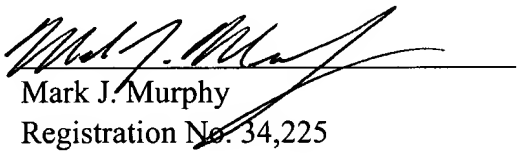
For at least the above-stated reasons, it is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any further fee is due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: October 31, 2002



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Marked-up copy of the claims as amended:

IN THE CLAIMS:

Please amend the claims as follows:

1. (Fifth Amendment) A semiconductor device comprising a plurality of MOSFETs formed in a single crystal semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region; and

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region and the source region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region[,].

[wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein the second impurity is introduced with a diagonal direction in a range of

45°±3° with respect to a surface of the single crystal semiconductor substrate.]

29. (Third Amendment) A semiconductor device comprising a plurality of MOSFETs formed in a single crystal semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region and the source region;

a pair of LDD regions, wherein one of the pair of LDD regions is formed between the source region and the channel forming region while the other of the pair of LDD regions is formed between the channel forming region and the drain region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region[,].

[wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the second concentration of the impurity in the channel forming region is

in a range of 1 x 10^{16} to 1 x 10^{17} atoms/cm^3,

wherein the second impurity is introduced with a diagonal direction in a range of 45°±3° with respect to a surface of the single crystalline semiconductor substrate.]

42. (Third Amendment) A semiconductor device comprising at least a CMOS circuit including an n-channel MOSFET and a p-channel MOSFET each being formed in a single crystal semiconductor substrate,

said n-channel MOSFET comprising:

a first source region and a first drain region each comprising a first n-type impurity;

a first channel forming region being formed between the first source region and the first drain region;

a first impurity region including a first p-type impurity and being formed under the first channel forming region and the first source region;

said p-channel MOSFET comprising:

a second source region and a second drain region each comprising a second p-type impurity;

a second channel forming region being formed between the second source region and the second drain region;

a second impurity region including a second n-type impurity and being formed under the second channel forming region[,].

[wherein each of the first p-type and the second n-type impurities is introduced from

a direction of the < 1 1 0 > axis with respect to the single crystal semiconductor substrate, so that each of the first p-type and the second n-type impurities is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein a concentration of the first p-type impurity in the first impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3,

wherein a concentration of the first p-type impurity in the first channel forming region is in a range of 1 x 10^{16} to 1 x 10^{17} atoms/cm^3

wherein a concentration of the second n-type impurity in the second impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3,

wherein a concentration of the second n-type impurity in the second channel forming region is in a range of 1 x 10^{16} to 1 x 10^{17} atoms/cm^3,

wherein each of the first p-type and the second n-type impurities is introduced with a diagonal direction in a range of 45°±3° with respect to a surface of the single crystal semiconductor substrate.]

Please add the following new claims:

56 (New). An EL display device comprising:

a plurality of MOSFETs formed in a single crystal semiconductor substrate, each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region; and

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.

57 (New). An EL display device according to claim 56,

wherein the first n-type impurity is arsenic,

wherein the second n-type impurity is phosphorus, and

wherein each of the first and second p-type impurity is boron.

58 (New). An EL display device according to claim 56, wherein the EL display device is incorporated into at least one selected from the group consisting of a cellular phone, a personal handy phone system and a portable computer.

59 (New). An EL display device according to claim 56, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.